

Amendments to the Drawings

The attached replacement sheet of drawings includes changes to Figure 7 and replaces the original sheet including Figure 7. In particular, Figure 7 has been labeled "Prior Art" as requested by the Examiner.

Attachments following last page of this Amendment

Replacement Sheet (1 page)

REMARKS

In response to the non-final Office Action of July 6, 2007, applicants ask that all claims be allowed in view of the amendments to the claims and the following remarks.

Claims 1-29 are now pending, of which claims 1-3 and 8 are independent. Claims 1-3 and 8 have been amended. Support for the amendments may be found in the originally filed application at least at page 4, lines 7-12; page 7, lines 27-30; and FIG. 1. No new matter has been introduced.

Objections to the Specification and Drawings

In response to the Examiner's objection to the specification, applicants have amended the abstract as shown above. The amendment is believed to address the concerns raised by the amendment. Accordingly, withdrawal of this objection is requested.

In response to the Examiner's objection to Figure 7, applicants have amended Figure 7. The amendment is believed to address the Examiner's concern. Accordingly, withdrawal of this objection is requested.

Claim Rejections—35 U.S.C. §102

Claims 1, 2, 4, 8, 14, 26, 27, and 29

Claims 1, 2, 4, 8, 14, 26, 27, and 29 have been rejected as being anticipated by U.S. Patent Application Publication No. 2001/0002703 (Koyama). Applicants request reconsideration and withdrawal of this rejection because Koyama does not describe or suggest that a gate electrode of a first transistor is connected to a second power line and a potential of the gate electrode of the first transistor is fixed, as recited in amended independent claims 1, 2, and 8.

In Koyama, a source or a drain region of a power source controlling transistor 112 is connected to an electroluminescence element 111, and a gate electrode of the power source controlling transistor 112 is connected to a power source control line 113 (which is one of the control lines C1 to Cn). See Koyama at ¶¶ 0115 and 0117 and FIGS. 2 and 3. The power source controlling transistor 112 is turned on by an external switch 117, which is connected to the

power source control line 113. See Koyama at ¶ 0131. In one aspect of Koyama, a source or a drain region of a power source control transistor 1009 is connected to an electroluminescence element 1006, and the gate electrode of the power source control transistor is connected to the power source control line 1010. See Koyama at ¶ 0148 and FIGS. 7A and 7B.

The Office Action equates Koyama's power source controlling transistor 112 (or 1009) with the recited first transistor. See Office Action at page 9, lines 8-9. However, rather than having a fixed potential, the gate of the power source controlling transistor 112 is connected to the external switch 117 through the power source control line 113 such that the potential of the gate changes so that the transistor 112 may be turned on by the external switch 117.

Accordingly, Koyama does not describe or suggest a first transistor having a gate electrode that is connected to a second power line and has a fixed potential, as recited in amended claims 1, 2, and 8.

For at least these reasons, applicants request reconsideration and withdrawal of the rejection of claims 1, 2, and 8 along with their dependent claims.

Claims 1-29

Claims 1-29 have been provisionally rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0252565 (Yamazaki '565). Applicants request reconsideration and withdrawal of this rejection because Yamazaki '565 does not describe or suggest a first transistor having a gate electrode that is connected to a second power line and has a potential that is fixed, as recited in amended claims 1-3 and 8.

In Yamazaki '565, a pixel included in a light emitting device includes a light emitting element 404, a switching transistor 401, a driving transistor 402, a current control transistor 403, and an erasing transistor 406 to erase an electrical potential of a video signal that is written in. See Yamazaki '565 at ¶¶ 0042-0043. One of the source and the drain of the switching transistor 401 is connected to the gate of each of the driving transistor 402 and the current control transistor 403. See Yamazaki '565 at ¶ 0044.

The Office Action equates the driving transistor 402 with the recited first transistor. See Office Action at page 10, lines 20-22. However, there is no indication that a potential of the gate of the driving transistor 402 is fixed. For example, the potential is varied in an erasing period, where the potential of a power supply line is supplied to the gate of the driving transistor 402 via the erasing transistor 406. See Yamazaki '565 at ¶¶ 0043 and 0046.

Accordingly, Yamazaki '565 does not describe or suggest a first transistor having a gate electrode that is connected to a second power line and has a potential that is fixed, as recited in amended claims 1-3 and 8.

For at least these reasons, applicants request reconsideration and withdrawal of the rejection of claims 1-3 and 8 along with their dependent claims.

Claim Rejections—35 U.S.C. § 103

Claims 3, 15, and 28

Claims 3, 15, and 28 have been rejected as being unpatentable over Koyama in view of U.S. Patent Application Publication No. 2002/0113760 (Kimura). Applicants request reconsideration and withdrawal of this rejection because neither Koyama, Kimura, nor any proper combination of these references describes or suggests a first transistor having a gate electrode that is connected to a second power line and has a potential that is fixed, as recited in amended claim 3.

As discussed above with respect to claims 1, 2, and 8, Koyama does not describe or suggest a first transistor arranged in this manner. Kimura, which is cited as showing a fourth transistor for forcing the light-emitting element into a non-emission state, does not remedy the failure of Koyama to describe or suggest this feature.

Claim 17

Claim 17, which depends from claim 3, has been rejected as being unpatentable over Koyama in view of Kimura and U.S. Patent No. 6,207,969 (Yamazaki '969). Yamazaki '969

does not remedy the failure of Koyama and Kimura to describe or suggest the subject matter of claim 3. Accordingly, applicants request withdrawal of this rejection.

Claims 5, 11, and 16

Claims 5, 11, and 16, which depend from one claims 1, 2, and 8, have been rejected as being unpatentable over Koyama in view of Yamazaki '969. As indicated above, Yamazaki '969 does not remedy the failure of Koyama to describe or suggest the features of claims 1, 2, and 8. Accordingly, applicants request withdrawal of this rejection.

Claim Rejections—Nonstatutory Obviousness-type Double Patenting

Osame '586

Claims 1-29 have been rejected for obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 7,173,586 (Osame '586). Applicants request reconsideration and withdrawal of this rejection because claims 1-10 of Osame '586 do not recite a first transistor having a gate electrode that is connected to a second power line and has a potential that is fixed, as recited in amended claims 1-3 and 8.

Osame '934 in view of Koyama

Claims 1-29 also have been rejected for obviousness-type double patenting as being unpatentable over claims 1-40 of U.S. Patent No. 7,141,934 (Osame '934) in view of Koyama. Applicants request reconsideration and withdrawal of this rejection because claims 1-40 of Osame '934 do not recite a first transistor having a gate electrode that is connected to a second power line and has a potential that is fixed, as recited in amended claims 1-3 and 8, and because, as discussed above, Koyama also fails to do so.

Fukumoto in view of Koyama

Claims 1-29 also have been rejected for obviousness-type double patenting as being unpatentable over claims 1-40 of U.S. Patent No. 7,122,969 (Fukumoto) in view of Koyama.

Applicants request reconsideration and withdrawal of this rejection because claims 1-40 of Fukumoto do not recite a first transistor having a gate electrode that is connected to a second power line and has a potential that is fixed, as recited in amended claims 1-3 and 8, and because, as discussed above, Koyama also fails to do so.

Copending Application No. 10/840,611

Claims 1-29 also have been provisionally rejected for obviousness-type double patenting over claims 1-52 of copending Application No. 10/840,611. Without conceding obviousness, applicants request that this provisional rejection be held in abeyance until the claims of both the present application and those in Application No. 10/840,611 are otherwise held to be allowable.

Yamazaki '565 in view of Koyama

Claims 1-29 have been provisionally rejected for obviousness-type double patenting over claims 1-22 of Yamazaki '565 in view of Koyama. Without conceding obviousness, applicants request that this provisional rejection be held in abeyance until the claims of both the present application and those in Yamazaki '565 are otherwise held to be allowable.

Conclusion

Applicants submit that all claims are in condition for allowance.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Pursuant to 37 CFR §1.136, Applicants hereby petition that the period for response to the Office Action dated July 6, 2007, be extended for one month to and including November 6, 2007.

Fees in the amount of \$120 in payment for the Petition for Extension of Time fee are being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. No additional fee is believed due. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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FIG. 7 (PRIOR ART)

